Design and Measurement of Very High Bitrate Digital ICs Fabricated in InP HBT Technology

A. Konczykowska, S. Blayac, F. Jorge, M. Riet, V. Puyal and J. Godin

Alcatel R&I/OPTO+, Route de Nozay, F-91461 Marcoussis, France

Abstract — **In this paper we present various design aspects of very high bitrate ICs and in particular electrical simulation and transistor modelling. Circuits are fabricated in a self-aligned InP DHBT technology. High speed selector design is used as illustration. Circuit measurements show excellent operation at 80 Gb/s (measurement set-up limitation). Circuit operation as 40 Gb/s NRZ to RZ converter was also characterised.**

I. Introduction

With the progress of semiconductor technologies based both on specific materials and on proper scaling of devices, higher operation bitrates can be contemplated for Electrical Time Division Multiplex (ETDM). The realisation of ICs necessary for such systems implies not only a high performance technology, but also specific design methodology including layout and packaging aspects at early stages of the design flow. Measurement of such high speed circuits also presents important challenges. One of the circuits operating at very high bitrate is a selector circuit. Selector is the core part of a multiplexer which is an important element of ETDM system. High speed multiplexers are also necessary for measurement setups to provide high bitrate signals needed for characterisation of such ICs as D-Flip Flops or demultiplexers.

High speed selectors and multiplexers have been fabricated in SiGe HBT [1], InP HEMT [2-3] and HBT [4-5] technologies.

In this paper we present the InP DHBT technology used for circuit fabrication (section II), some simulation aspects including novel modelling of III-V semiconductor devices (section III), the selector design (section IV) and measurement results (section V).

II. Technology

The InP/InGaAs Double Heterojunction Bipolar Transistor (DHBT) technology presents several attractive aspects for the fabrication of high speed circuits.

Very high frequency characteristics are due to excellent electron transport properties of InP and InGaAs; the small bandgap of InGaAs base results in a low turn-on voltage, which means a potential for low power consumption; the double heterojunction gives a high breakdown voltage, necessary for large signal applications such as optical modulator drivers; finally, the vertical technological process yields a very good built-in threshold voltage uniformity, very convenient for differential bipolar logics such as CML and ECL.

An InP/InGaAs self-aligned DHBT technology has been developed at OPTO+ [6]. The transistors exhibit a high breakdown voltage (BV_{CE0} >7 V) as the result of the double heterojunction structure. 150-180 GHz F_t and 210-220 GHz F_{max} are currently obtained on circuit-oriented devices at a current density about 2 mA/μm². Three Ti/Au interconnection levels, TaN resistors, MIM capacitors and spiral inductors are available to realise the circuit layout.

In Fig. 1 Ft and Fmax frequencies for 2x3 μm² and 2x10 μm² emitter transistors are compared vs. collector current. As you can notice Ft above 100 GHz and Fmax over 170 GHz are achieved for currents of 2 mA for small transistors. This means that low power high frequency operation can be contemplated.

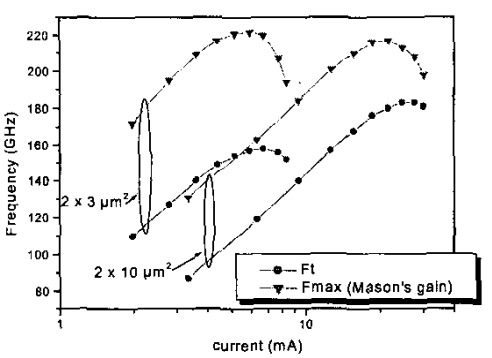

Fig. 1 Ft and Fmax for 2x3 and 2x10 μm² emitter transistors

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III. Circuit Simulation and Modeling Aspects

The design of ICs operating at very high bitrates needs adequate methodology on electrical as well as on layout level.

To evaluate correct operation and especially eye-opening (rise and fall times and time jitter) precise transient simulations on sufficiently long time intervals are necessary. These simulations should be based on correct models for both active, passive and parasitic elements.

Particular attention has been paid to transistor models. The limitations of popular Gummel-Poon bipolar transistor model when applied to III-V compound transistors have been pointed out in many occasions. Some techniques to overcome these difficulties were presented in [7]. But with the increase of the operating speed the limitations of this approach become unacceptable. E.g. the impossibility to model correctly Cbc dependence on bias conditions and in particular the exponential growth in high-current regime may be very misleading. In Fig.2 we compare Cbc values extracted from measurement and those of Gummel-Poon model which are constant with Ic current .

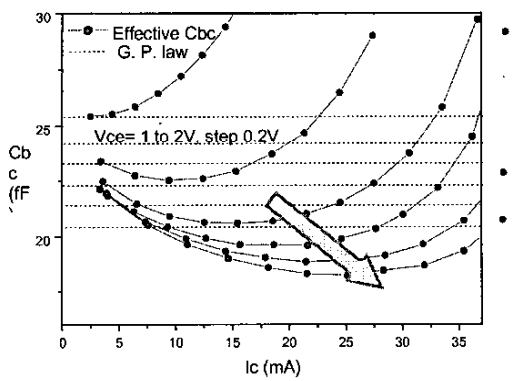


Fig. 2 Cbc in function of Ic for different Vce: extracted (solid) and Gummel-Poon law (dotted lines)

Most important features that should be taken into account by transistor models in order to accurately represent large signal operation at high bitrates are:

- Current dependence of τ_f due to electric field profile modulation;
- Voltage dependence of τ_f due to intervalley scattering;
- Exponential dependence of C_{bc} in high-current regime due to electron accumulation;
- Heterojunction-specific "saturation" static regime so that access resistances are not overestimated.

In the design presented below, we used the IIBT model [8] which allows to implement the most important features necessary for the correct simulation of high speed circuits.

IV. Circuit Design

In this section we present the design aspects of high speed selector.

A. Electrical design

The selector block diagram is presented in Fig. 1. The two data (D1 and D2) are single ended and converted by the input buffers to differential ones. Clock buffer is realised with two ECL stages. It amplifies the clock signal and allows to balance the time slots between D1 and D2. The buffer is also used to modify the pulse width when the selector is used as a NRZ to RZ signal converter. Circuit core is realised with E^2CL differential pairs. Small transistors (2x3 μm^2) with 1.3 $mA/\mu m^2$ current density are used resulting in low power consumption. Output buffer uses CML structure which results (for the realised circuit) in a limited output swing.

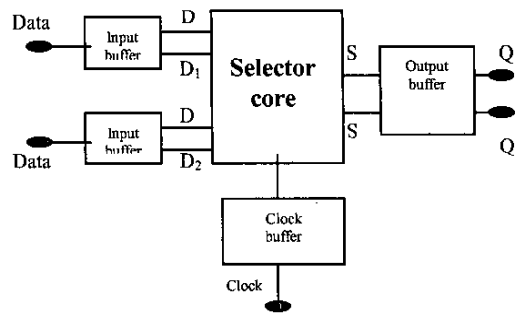


Fig. 3. Selector bloc or schematic

In order to better estimate the selector operation in the real environment, the circuit was simulated using the data registered from the measurement equipment. In Fig. 4 selector simulation results are presented. The real input signal at 40 Gb/s is on the top, while the 80 Gb/s selector output is in the bottom. The time jitter of the output signal is reduced compared to the important jitter of the input signal. Further reduction can be expected with the full MUX realisation when the two input signals will be fed to the selector after reshaping and resynchronisation with the Master-Slave (MS) and MSS stages. The presented simulation was realised with the redesigned output buffer, based on the ECL architecture, with the 600 mV output swing. This new version of the circuit will be soon fabricated.

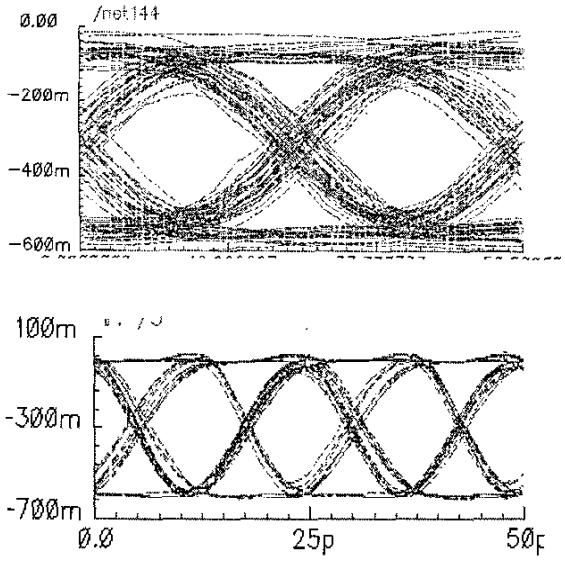


Fig. 4 Selector eye-diagram simulation (top) 40 Gb/s input (bottom) 80 Gb/s output

B. Layout design

Signal part of the layout is compacted to shorten high frequency paths. Signal lines (two data and clock) are fed via matched 50 Ω CPW lines. Similarly output signal and its complementary are connected to output pads with 50 Ω CPW lines. DC bias connections are decoupled on wafer with RC circuits. The chip dimensions are 1.4×1.6 mm². A microphotograph of selector layout is presented in Fig. 5.

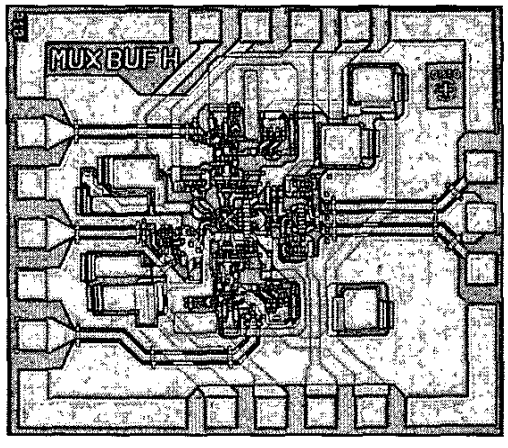


Fig. 5 Microphotograph of fabricated selector

V. SELECTOR MEASUREMENTS

The measurement of very high speed ICs (40-80 Gb/s) requires adequate measurement instruments as well as a special care in preparing the characterisation set-up. The used measurement set-up is composed as follows: a pseudo-random bit-pattern generator (PRBG) provides a data signal up to 20 Gb/s and its complementary. One data stream is delayed and multiplexed with the other, using a 40 Gb/s 2:1 MUX. Two complementary data streams at 40 Gb/s are similarly fed to the selector inputs through delay lines with different settings.

65 GHz probes were used at the circuit output. Measurements were realised with a remote sampling head (70 GHz) and very short cables. This remote head allows to avoid degradations due to long cables and offers the bandwidth (70 GHz) necessary for such high speed measurement. The use of a precision timebase module allows to characterise precisely the time jitter of DUT.

In Fig. 6, the eye diagram of the output signal (colour graded) at 80 Gb/s is presented. The vertical eye opening is 67 %, while the horizontal eye opening is 73 % corresponding to a 0.56 ps rms time jitter. 20-80% rise and fall times are about 6 ps. The output swing is 150 mV, due to the CML architecture of the output buffer.

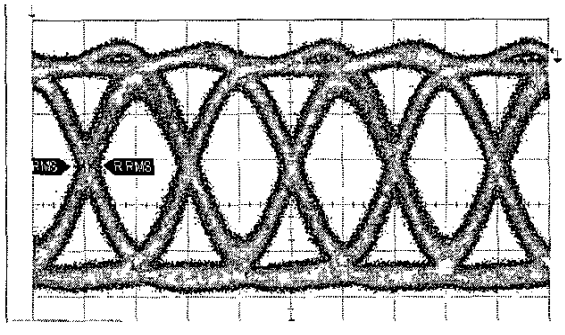
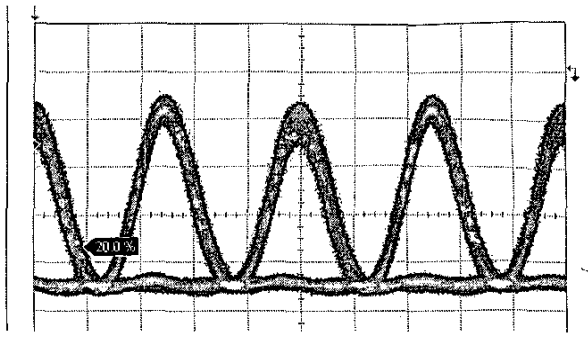
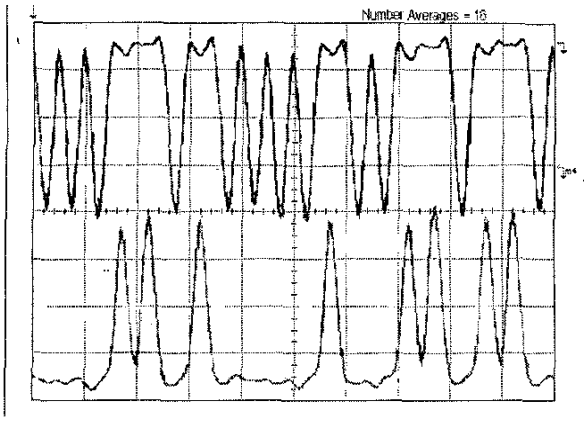


Fig. 6. 80 Gb/s selector eye diagram (6.3 ps/div)

By applying constant signal on one of the selector inputs, we achieve the NRZ to RZ conversion at 40 Gb/s. In Fig. 7 (a) the RZ eye diagram is presented. The pulse width is adjustable. In Fig. 7 (b) the RZ output waveform segments are presented. The 40 Gb/s input signal is applied to one input. These outputs correspond to the sequence: 0001101000010011011O (bottom) and its complementary (top). The horizontal scale is 50 ps/div (two bits/division). Rise and fall times are less than 5.5 ps.



(a)



(b)

Fig. 7. 40 Gb/s NRZ to RZ conversion
(a) RZ eye diagram (10 ps/div)
(b) RZ waveform segments (50 ps/div)

VI. Conclusion

In this paper we discussed some aspects of the high speed circuit design, and in particular modelling issues of InP DHBTs. The design, fabrication and measurement of the high quality selector was discussed in detail. For this circuit, 80 Gb/s operation with significantly improved quality, compared to previously reported, was measured. Clear eye with 67 % vertical and 73 % horizontal opening has been observed. 0.56 ps rms time jitter and rise and fall times about 6 ps were measured. Circuit operation as NRZ to RZ converter has been characterised.

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